REMARKS/ARGUMENTS

This paper responds to the Office Action of April 26, 2004.

Applicant respectfully requests examination of the application.

I. Preliminary Amendment and Formal Drawings

A Preliminary Amendment (with a Replacement Specification) and Formal Drawings were filed in February 2002. Neither the Amendment nor the Drawings are acknowledged in this Office Action. Applicant requests confirmation that this Amendment and Drawings were received and entered.

II. Information Disclosure Statements

Paragraph 1 of the Office Action is not understood.

Paragraph 1 of the Office Action states that references supplied in several Information Disclosure Statements were not considered "because [they] do not include a concise statement of the relevance ... of each patent listed that is not in the English language."

The Office Action gives no explanation for the failure to consider the references that are in the English language. Applicant requests that all English language references be considered pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98. For the Examiner's convenience, all references to be made of record are presented in numerical order, in one consolidated IDS and set of Forms 1449, filed herewith.

III. § 112 ¶ 2 question

Paragraph 3 of the Office Action is not understood. It purports to reject claim 24 under § 112 ¶ 2, but points to no particular language of claim 24, let alone two or more possible interpretations that one of ordinary skill might assign to that language. No rejection exists. Nonetheless, Applicant offers the following explanation in order to advance prosecution.

Claim 19 recites "an instruction set in which an interpretation of an instruction depends on a processor mode not expressed in the binary representation of the instruction." One typical such instruction set is the Intel X86 instruction set, which has a number of different mode bits. These mode bits dramatically alter the behavior of instructions. For example, a single ADD instruction may add 8, 16 or 32 bits – a single instruction may perform three different operations, depending on the mode bits that are "not expressed in the binary representation of the instruction." (These modes are described, for example, in the Intel Architecture manuals cited on the accompanying IDS.)

Claim 24 recites "a binary translator configured to translate programs coded in the instruction set in which an interpretation of an instruction depends on a processor mode not expressed in the binary representation of the instruction, being a first instruction set architecture, into instructions of a second instruction set architecture." That is, claim 24 recites a binary translator that is confronted with the difficult task of performing an accurate translation of a program that is expressed in an instruction set where instructions cannot be taken at face value.

Claim 24 is neither vague nor indefinite. Rather, claim 24 is directed to a problem that had no obvious solution before Applicant's invention.

IV. Double Patenting

Paragraph 4 of the Office Action is not understood.

First, the Office Action does not use any of the approved form paragraphs from Chapter 800 of the MPEP. It mixes reasoning and case citations that relate to statutory same-invention type double patenting and obviousness-type double patenting, without indicating which one is thought to apply. Because of the ambiguous statement of grounds, Applicant is unable to determine the appropriate responsive action.

Second, double patenting is an analysis that must be conducted on a claim-by-claim basis. The double-patenting form paragraphs and each subsection of MPEP § 804 require the identification of particular pairs of claims, and a showing that one particular claim in the pending application cannot be literally infringed without literally infringing one corresponding particular claim the other application, and *vice-versa*. For example, MPEP § 804(B)(1) instructs that when

making an obvious-type double patenting analysis, the following factual inquiries must be set forth:

> (A) Determine the scope and content of a patent claim [singular] and the prior art relative to a claim [singular] in the application at issue;
>
> (B) Determine the differences between the scope and content of the patent claim [singular] and the prior art as determined in (A) and the claim [singular] in the application at issue;

Because the Office Action never compares a particular claim of this application to a particular claim of the '852 application, no double-patenting rejection exists.

Third, because of these two failures to clearly state a rejection, no double-patenting rejection exists.

Fourth, Applicant further notes that no double patenting rejection could be raised. For example, each of the independent claims of application serial no. 09/330,852 recites one or both of the following limitations:

- recording profile information concerning the execution of the program, the profile information recording of the address of the last byte of at least one instruction (claims 1, 2 and 24)
- ... the program being coded in an instruction set in which an interpretation of an instruction depends on a processor mode not expressed in the binary representation of the instruction; [and] recording profile information ... efficiently tailored to annotate the profiled binary code with sufficient processor mode information to resolve mode-dependency in the binary coding. (claims 1, 34 and 46).

In contrast, none of the independent claims of this application recite either of these limitations. As requested in paragraph 4 of the Office Action, "a clear line of demarcation" has been maintained between the claims of the applications. No double-patenting rejection is warranted.

V. Claims 1 and 19

Claim 1 recites as follows:

> 1. A method, comprising:
>
> during a profiled interval of an execution of a program on a computer, recording profile information describing the execution, without the program having been compiled for profiled execution, the program being coded in an instruction set in which an interpretation of an instruction depends on a processor mode not expressed in the binary representation of the instruction, the recorded

> profile information describing at least all events occurring during the profiled execution interval of the two classes:
>
> a divergence of execution from sequential execution;
>
> a processor mode change that is not inferable from the opcode of the instruction that induces the processor mode change taken together with a processor mode before the mode change instruction;
>
> the profile information further identifying each distinct physical page of instruction text executed during the execution interval.

First, the Office Action fails to make any comparison of the word "physical" to the reference, and thus raises no rejection.

Second, the Office Action is incomplete because it fails to make a proper showing of inherency. Any rejection based on inherency is governed by MPEP § 2112:

> **2112 Requirements of Rejection Based on Inherency; Burden of Proof**
>
> ...
>
> **IV. EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY**
>
> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. ...
>
> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art."

The Office Action makes the bald statement that Heisch '033 "inherently includes pages." The Office Action provides no "basis in fact and/or technical reasoning." Because the Office Action is incomplete, no rejection exists.

Third, Heisch '033 must work with virtual addreses, not "physical" addresses, as recited in claim 1. For example, all of the program events he discusses – branches, basic blocks, tracebacks, function calls, etc. – operate on the basis of virtual addresses, not physical addresses. If Heisch tried to base his system on physical addresses, it wouldn't work – parts of the system that rely on the stability of virtual addresses would be "fooled" as parts of a program are moved from one physical address to another by the virtual memory system.

Claim 19 recites similar language, and is patentable for similar reasons.

Claims 2-18 and 20-30 are dependent on claims 1 and 19, and allowable therewith. In addition, they recite other patentable features that further distinguish the art.

VI. Claims 14 and 28

Paragraph 8 of the Office Action states that Heisch and Roediger are combinable "for the same reasons utilized by Y..." The reference to "Y" is not understood. Similarly, it appears that the reasons stated may be "boilerplate" form language, not reasoning particularized to these claims and references.

If any obviousness rejection is thought to apply, Applicant requests the three showings set out at MPEP § 2143-2143.03: Motivation to modify or combine, reasonable expectation of success, and every element taught or suggested. Without these three *prima facie* showings, no obviousness rejection can exist.

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. Enclosed is Petition for Extension of Time for one month. In the event that any extension of time is required, Applicant petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-09-4016.

Respectfully submitted,

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Dated: August 20, 2004

By: _____

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